

IN THE CLAIMS

1. (Currently Amended) A semiconductor device comprising:

a ~~plurality of~~ memory block circuits addressed ~~designated by ND (ND = 2^{NA}) address expressed~~ by a binary address of NA bits; and

a defect address storing circuit including ND (ND = 2^{NA}) storage elements for storing NS (NS = two ~~and over~~ or more) defect addresses in relation to a plurality of defects in the ~~plurality of~~ memory block circuits,

wherein the NS defect addresses from said binary address of NA bits are addresses which are different from each other ~~selected from the ND address~~, and

each of the ND storage elements stores ~~a first logical state or a second logical state~~ in one bit.

2. (Currently Amended) A semiconductor device according to claim 1,

wherein an initial value of each of the ND storage elements is in a ~~the~~ first logical state and the NS storage elements in the ND storage elements are programmed into a ~~the~~ second logical state, thereby storing the NS defect addresses.

3. (Currently Amended) A semiconductor device according to claim 1,

wherein each of the NS defect addresses is expressed by a decoded address of ND bits,

wherein one bit of the decoded address of ND bits is in a the second logical state and the other bits are in a the first logical state, which is different from said second logical state, and

wherein the bits in the second logical state of the NS defect addresses are sequentially programmed into the ND storage elements in accordance with the order starting from the an address having a ~~smaller number~~ first value to ~~the an~~ address having a ~~larger number~~ second value larger than said first value.

4. (Original) A semiconductor device according to claim 1,

wherein $NS > (2^{NA}) / (NA + 1)$ is satisfied.

5. (Original) A semiconductor device according to claim 1,

wherein each of the plurality of memory circuits includes a plurality of memory cells provided at intersecting points of a plurality of word lines and a plurality of bit lines and

wherein the number of the plurality of memory circuits is ND.

6. (Original) A semiconductor device according to claim 5, further comprising:

a flexible column redundancy circuit for repairing a defect in the bit lines in the plurality of memory circuits,

wherein the defect address storing circuit is included in the flexible column redundancy circuit, and

wherein the ND storage elements store addresses of the plurality of memory circuits relating to a defect.

7. (Currently Amended) A semiconductor device according to claim 1,

wherein each of the ND storage elements is a fuse circuit for storing a ~~the~~ first logical state as an initial value and storing a ~~the~~ second logical state by being programmed.

8. (Currently Amended) A semiconductor device comprising:

a ~~plurality of~~ memory circuits having designated by ~~ND (ND = 2^{NA}) address expressed by~~ binary addresses of NA bits; and

a defect address storing circuit including (ND + NS - 1) storage elements for storing NS (NS = two or more ~~and over~~) defect addresses in relation to a plurality of defects in the ~~plurality of~~ memory circuits,

wherein the NS defect addresses can be selected ~~in~~
~~such a manner~~ so that the same address selected from the ND
addresses may be repeated,

wherein each of the $(ND + NS - 1)$ storage elements
stores ~~a first logical state or a second logical state in one~~
a bit, and

wherein NS is larger than ND.

9. (Original) A semiconductor device according to claim
8,

wherein the $(ND + NS - 1)$ storage elements are
divided into a first group of ND storage element as a first
array and second group of $(NS - 1)$ storage elements as a
second array,

wherein the first group of NS storage elements store
independent addresses which are different from each other in
the ND addresses, and

wherein the second group of $(NS - 1)$ storage
elements store the number of duplex selection of an address
which is repeated in the independent addresses.

10. (Currently Amended) A semiconductor device
according to claim 9,

wherein each of the NS defect addresses is expressed
by a decoded address of ND bits,

wherein one bit in the ND bits of the decoded address is in a ~~the~~ second logical state and the other bits are in a ~~the~~ first logic stage, different from said second logical state, and

wherein the bits in the second logical state of the NS defect address are sequentially programmed into the first group of ND storage elements in accordance with the order from the address having a ~~smaller number~~ small value to the address having a ~~larger number~~ large value.

11. (Original) A semiconductor device according to claim 8,

wherein $NS > ((2^{NA}) + 1)/NA$ is satisfied.

12. (Original) A semiconductor device according to claim 8,

wherein each of the plurality of memory circuits has a plurality of memory cells provided at intersecting points of a plurality of word lines and a plurality of bit lines, and

wherein the number of the plurality of memory circuits is ND.

13. (Original) A semiconductor device according to claim 12, further comprising a flexible column redundancy circuit for repairing a plurality of defects, each defect is associated with a bit line in one of the plurality of memory circuits,

wherein the defect address storing circuit is included in the flexible column redundancy circuit, and

wherein the $(ND + NS - 1)$ storage elements store addresses of the plurality of memory circuits related to the plurality of defects.

14. (Currently Amended) A semiconductor device according to claim 13,

wherein each of the $(ND + NS - 1)$ storage elements is a fuse circuit for storing a ~~the~~ first logical state as an initial value and storing a ~~the~~ second logical state by being programmed.

15. (Original) A semiconductor device comprising:

a plurality of memory blocks each having a plurality of memory cells provided at intersecting points of a plurality of bit lines and a spare bit line which cross a plurality of word lines;

a plurality of column selection lines, each provided for one of the plurality of bit lines of the plurality of memory blocks;

a spare column selection line provided for the spare bit line of the plurality of memory blocks; and

a redundancy circuit having an input node to which an access address including a first access information for designating one of the plurality of memory blocks and a second

access information for designating one of the plurality of column selection lines is supplied, a defect address storing circuit for storing a plurality of defect addresses, and an output node which is coupled to the spare column selection line to make the spare column selection line active when the access address coincides with the plurality of defect addresses,

wherein the defect address storing circuit further includes a first storage set for storing a first information to designate one the plurality of column selection lines related to a first defect, a second storage set for storing a second information for designating one of the plurality of column selection lines related to a second defect, and a third storage set for storing a third information for designating one of the plurality of memory blocks related to the first defect and a fourth information for designating another one of the plurality of memory blocks related to the second defect, and

wherein the third storage set has a plurality of storage elements of the number equal to the number of the plurality of memory blocks, which are provided as an array and stores the third and fourth information by the plurality of storage elements.

16. (Original) A semiconductor device according to claim 15,

wherein one of the plurality of memory blocks in which the first defect is included is designated by programming corresponding one of the plurality of storage elements,

wherein another one of the plurality of memory blocks in which the second defect is included is designated by programming another corresponding one of the plurality of storage elements,

wherein the storage element programmed first in the array of the plurality of storage elements is associated with the first storage set, and

wherein the storage element programmed second in the array of the plurality of storage elements is associated with the second storage set.

17. (Original) A semiconductor device according to claim 15,

wherein the defect address storing circuit further includes a fourth storage set for storing information to select one or plural memory blocks which is/are neighboring one of the plurality of memory blocks selected by the third storage set in relation to the first defect.

18. (Original) A semiconductor device according to claim 17, further comprising a plurality of sense amplifiers which are provided between one the plurality of memory blocks and another neighboring one of the plurality of memory blocks and are commonly used by the plurality of bit lines in one of the plurality of memory blocks and another neighboring one of the plurality of memory blocks, and

wherein the first defect is a defect related to one of the plurality of sense amplifiers coupled to one of the plurality of bit lines related to one of the plurality of column selection lines.

19. (Original) A semiconductor device according to claim 15,

wherein the redundancy circuit further comprises a shifter having a plurality of first input nodes to which the first access information is inputted in a decoded address format, a plurality of first output nodes of the number smaller than the number of the plurality of first nodes, and a switch circuit for setting a plurality of logical connecting paths between the plurality of first input nodes and the plurality of first output nodes,

wherein the plurality of logical connecting path are determined by the information stored in the plurality of storage elements in the third storage set.

20. (Original) A semiconductor device according to claim 19,

wherein one of the plurality of first output nodes determines whether the result of comparison between the first information stored in the first storage set and the first access information is made valid or not, and

wherein another one of the plurality of first output nodes determines whether the result of comparison between the second information stored in the second storage set and the first access information is made valid or not.

21. (Original) A semiconductor device according to claim 15,

wherein the first storage set includes a plurality of first storage elements and stores the first information in a binary address format,

wherein the second storage set includes a plurality of second storage elements and stores the second information in a binary address format, and

wherein the plurality of storage elements in the third storage set store the third and fourth information in a decoded address format obtained by decoding the information in the binary address format.

22. (Original) A semiconductor device according to claim 15, further comprising a plurality of address input

terminals to which a row address and a column address are supplied by an address multiplexing method,

wherein the first access information is obtained from the row address and the second access information is obtained from the column address, and

wherein the semiconductor device is a dynamic random access memory.

23. (Once Amended) A semiconductor device according to claim 15,

wherein each of the plurality of storage elements is a fuse circuit which stores a ~~the~~ first logical state as an initial value and stores a ~~the~~ second logical state when being programmed.

Claims 24-35 (Canceled)